REMARKS

The comments of the applicant below are each preceded by related comments of the examiner (in small, bold type).

2. Claims 1-7, 26-29, 33-35, 37, 40, 41, 43, 45 and 57-60 have been allowed.

The Applicant thanks the Examiner for allowing claims 1-7, 26-29, 33-35, 37, 40, 41, 43, 45, and 57-60.

3. Claim 56 is objected to because of the following informalities: "programming agent" should be changed to "processing agent". Appropriate correction is required.

Applicant notes that Claim 56 currently recites "programming engine." The use of programming engines is supported by the specification. For example, the term "programming engines" can be found on page 3, lines 13 to 19 and page 9, lines 1 to 14 of Applicants' specification.

5. Claims 13, 16-21, 44 and 49-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Per claims 13, 49 and 52, the words "permitting" renders the claims' metes and bounds unclear, since the claims would appear to cover anything and everything that does not prohibit the actions from occurring.

Claims 13, 49, and 52 have been amended.

7. Claims 13, 16-19, 44, 49, 50, 52, 53, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singhal et al. [5,978,874] (hereinafter "Singhal"), in further view of Misra et al. [US 6,654,836 B1] (hereinafter "Misra").

Per claims 13, 49, 52, 55 and 56, Singhal teaches a system comprising: a plurality of memory resources [e.g., Data Out Buffer ("DOB") 186 and Data In Buffer ("DIB"), col. 29, lines 59-62; copy buffers or streaming 10 buffers, col. 16, lines 50-55] each memory resource being associated with a memory controller [189, fig. 3], a processing agent [180, fig. 2; Address Controller 180 generates control signals that are carried over path 190 to the Data Controller 140. Signal timings on the DataBus 70, the AddressBus/State Bus 60, the Arbitration Bus 80, and the Data ID Bus 90 are designed to permit such multiplex-partitioning of data and address paths, col. 6, lines 23-29] to access the memory resources; a single bus to push data from the memory resources to the processing agent; a push bus arbiter [col. 16, lines 62-65] to arbitrate use of the bus by the memory resources, the memory resources obtaining access to the bus based on arbitration by the push bus arbitrator; a single bus to receive data from the processing agent and to transfer the data to the memory resources; and a pull bus arbiter to arbitrate use of-the bus by the memory resources, the memory resources obtaining access to the bus based on arbitration by the pull bus arbiter.

Singhal does not teach a system and a method for arbitrating data between the processing agent [e.g.. Initiator] and the memory resource [e.g., Responder] using two different buses: a Push bus and a Pull bus; and unidirectionally transferring data from one of the memory resources to the processing agent through the push bus during a read phase, or unidirectionally transferring data from the processing agent to one of the memory resources through the pull bus during a write phase.

It would have been obvious for one having ordinary skill in the art at the time the invention was made to use two different buses for arbitrating data between the processing agent [e.g., Initiator] and the memory resource instead of a single bus in order to reduce number of turn-around cycles per bus, because the request and associated data are generally not sent on the same bus. Furthermore, the bandwidth in a two-bus connection is increased significantly over the single bus. The advantages of multiple buses considerably increase memory bandwidth and increase data throughput via multiple data passages.

Furthermore, Misra teaches a controller having separate parts to handle read and write operations [see Fig 3] and a shared unidirectional pull bus (write data bus) and a shared unidirectional push bus (read data bus) [see Fig 2] in order to allow the controller to perform read and write operations at the same time [see column 3, lines 45-50]. Misra further teaches a read data phase and a write data phase in which the read and write operations are performed [see Fig 4], and such phases are the result of having a bus controller/arbiter in order to regulate the transfer of data between two devices. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine Misra's teachings with those of Singhal for the above reasons. As a result of the combination, it is also made clear that the push bush only permits data to be sent from the memory resources and the pull bus only permits data to be sent from the processing agent as the buses are unidirectional. It is also clear that combining Misra's buses with Singhal's system would result in each board having separate read data bus and write data bus to the on board memory, while a shared read bus and a shared write bus which are common to the boards are used for making requests to each other. An arbiter must be present when there is a possibility of multiple requests contending for access to a shared bus, and when there is a possibility of multiple requests arriving at a receiver simultaneously. Therefore, combined Misra and Singhal clearly indicates that separate read data bus arbiter and write data bus arbiter must be present on each board.

It is also clear that claims 55 and 56 are already described but claims 13, 49, 52.

Singhal and Misra do not disclose and would not have suggested a unidirectional push bus to push data from the memory resources to the processing agent, and a unidirectional pull bus to receive data from the processing agent and to transfer the data to the memory resources, as recited in amended claim 13.

Singhal discloses a computer system having plug-in circuit boards 50-N that each includes CPU devices and on-board RAM (col. 6, lines 7-11). The CPU on each board can read data from the memory of any other board through a single bi-directional bus (col. 5, lines 34-37 and col. 7, lines 60-65). The Examiner appears to contend that the combination of Singhal and

Misra teaches the use of a shared read bus and a shared write bus that are common to the boards for making requests to each other.

The Applicant disagrees. Using unidirectional push and pull buses in Singhal's system would be much more complicated than using a bi-directional bus. It is unclear how the boards can share unidirectional push and pull buses when each board can access the memory of any other board. For example, how can boards 50-1 and 50-2 share a unidirectional push bus that allows data to be pushed from the memory of board 50-1 to the CPU of board 50-2, and from the memory of board 50-2 to the CPU of board 50-1? When the number of boards increases, sharing of unidirectional push and pull buses among the boards becomes even more problematic. Thus, there would be no motivation or suggestion to combine Misra with Singhal.

Claims 16-21 and 44 are allowable at least for the reasons discussed in claim 13. Claims 49-54 are allowable for analogous reasons given for claim 13.

Singhal does not disclose and would not have suggested a data processor that includes both a push bus arbiter and a pull bus arbiter, as recited in claim 55. Singhal does not disclose or suggest separate read and write buses, let alone a data processor that has separate push bus and pull bus arbiters.

What is missing in Singhal is also not disclosed or suggested in Misra. Misra discloses an arbiter 120 that is external to a processor core 110 (FIG. 1). Misra also discloses using one internal arbiter 342 that arbitrates read and write operations (FIG. 3). Misra does not disclose using separate push bus arbiter and pull bus arbiter within one data processor.

Claim 56 is allowable for analogous reasons given for claim 55.

All of the dependent claims are patentable for at least similar reasons as those for the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

An Information Disclosure Statement was filed on June 3, 2004. The Applicant respectfully requests that the Examiner consider the references cited in the Statement, and return an initialed Form 1449 for Applicant's records.

Please apply any charges or credits to deposit account 06-1050, reference 10559-618001.

Respectfully submitted,

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